CMOS reaches for 60GHz+ applications?

CMOS integrated circuit development has been full of surprises, more often than not wildly exceeding expectations. Dr Mike Cooke writes on developments designed to use the low-cost, highly integrated technology for extremely high radio frequency applications at tens of gigahertz.

In the very old days, complementary metal-oxide semiconductor (CMOS) technology was 'just digital'. For analog radio-frequency (RF) applications, designers had to look to the much more expensive silicon bipolar (possibly mixed with CMOS in BiCMOS) or III-V semiconductor technologies; then, as CMOS' frequency reach came within the suitable ranges, a number of RF technologies have become part of the CMOS empire. For frequencies of the order of gigahertz (GHz), CMOS RF applications are mainly short-range technologies such as Bluetooth and WiFi wireless networking, operating mainly at about 2.4GHz. In mobile phones (generally operating at 0.8–2.2GHz, but with some operating at ~0.4GHz), which need to transmit over longer ranges, the dominant semiconductor technology for power amplification is III-V due to the smaller components and to the better power efficiency achievable. However, manufacturers would love to have a lower-cost CMOS component.

NXP (formerly Philips Semiconductors) is one of those seeking a single-chip CMOS mobile phone. In 2007, the company acquired the cellular communications division of Silicon Labs, a developer of CMOS RF power amplifiers (PAs) with some take-up in China for very low-cost mobiles. However, the balance between cost, size and battery-life dictates that III-V components are generally preferred for this application at present.

On the other hand, low-noise amplifiers (LNA) for the receiver side are often integrated in CMOS in a single chip with the circuitry required to convert both ways, between digital signals of the baseband device and the modulated radio signal to and from the external network.

Having extended CMOS into many gigahertz-level RF applications, with new ones such as WiMAX (2.5–3.5GHz and other ranges) coming into view, researchers have in the past few years been looking beyond 10GHz for new CMOS RF applications.

On the one hand, the higher frequencies are expected to enable much higher data rate communication; but on the other hand, the range 10–100GHz is obscured by various forms of atmospheric absorption (Figure 1).

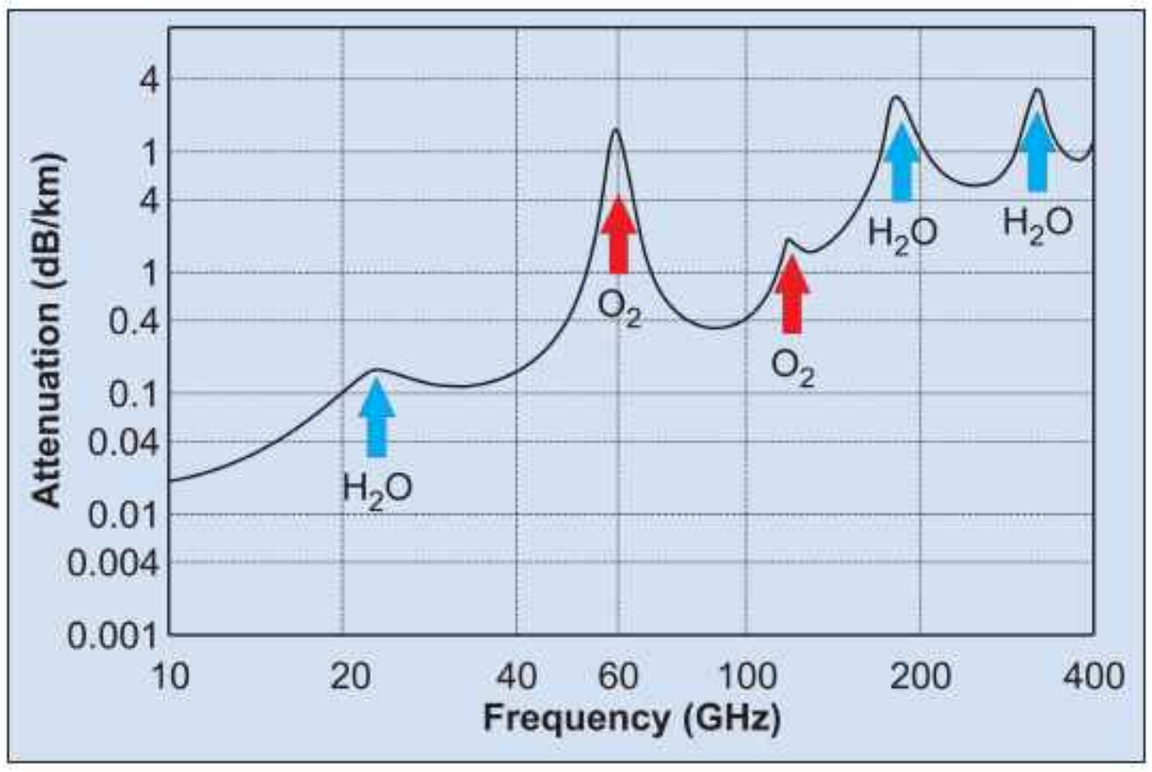

Figure 1. Average atmospheric absorption at sea level with T = 20°C, P = 760mm, H_2O = 7.5g/m^3.

One application that is planning to make a virtue out of absorption is wireless networking in the region of 60GHz. Up to now, this band's main use has been in satellite-to-satellite communication. The attraction, particularly for military/intelligence applications, is that this band is strongly absorbed by oxygen, making it practically impossible to eavesdrop on such communications from the ground. For wireless networking, the short range in oxygen makes interference from other networks less of a problem compared with lower-frequency systems, where complicated schemes can be needed to figure out which network is being used by a particular signal. In addition to oxygen, 60GHz signals are also blocked by walls and human skin (avoiding health concerns, it is argued).

While high data rates are desirable for most applications (where practical/cost effective), there are some new technologies where they are a necessity. One of these is the wireless communication of high-definition television (HDTV) signals. Compressed HDTV requires data rates that are about three to four times those of digital TV — about 15Mbit/s compared with 5Mbit/s for DVD quality. Also, 15Mbit/s is a rock-bottom figure: HD DVD or BluRay disks can need

up to 50Mbit/s; uncompressed signals used in studios and in some wall-mounted plasma displays can reach 1.4Gb/s. The high-definition multimedia interface (HDMI) standard requires data rates of up to 5Gbit/s and the newer DisplayPort 10.8Gbit/s. Although HDTV can be transmitted over 5GHz networks, the description is often 'and even', suggesting that the capability is at the limit, with very little wiggle room.

Proposals for 60GHz-band networking have bit rates of several Gb/s, with a range of up to 10 meters. This would be used to create wireless personal area networks (WPANs) and local area networks (WLANs), allowing wireless Gigabit Ethernet, laptop docking stations, mobile device synchronization (cellphones, iPods, MP3 players, cameras, handhelds/PDAs, etc.), broadband video distribution, and wireless Firewire (IEEE1394), USB 2.0, display and other peripheral connections. Such WPANs could be set up in offices, homes, hotel rooms, cafes and so on. Commercial kiosks in the street, airport, train station and so on could enable mobile downloads of DVDs to personal devices in seconds.

One strand of WPAN development is carried out under the IEEE802.15 standard, with the IEEE802.15.3c working group focusing on millimeter-wave (mm-wave) opportunities such as 60GHz. The term 'mm-wave' is commonly used to refer to the portion of the radio spectrum from about 30GHz up to 300GHz. The wavelengths of such radio waves cover the range from 10mm down to 1mm.

Another organization developing WPAN standards for 60GHz wireless is ECMA International, a body focused on Information and Communication Technology (ICT) and Consumer Electronics (CE). In February 2007, representatives met from the Electronics and Telecommunications Research Institute (ETRI) of Korea, Georgia Electronics Design Center (GEDC), Intel, IBM, Matsushita Electric Industrial (Panasonic), Newlans, Philips Semiconductors (now NXP), Samsung Electronics and Samsung Electro-Mechanics; a white paper describing a draft standard (TC48) was issued this February. The standard is designed to provide high-rate WPAN (including point-to-point) transport for bulk data transfer and multimedia streaming.

In addition, the WirelessHD standard plans to use the 60GHz band to stream high-definition multimedia content to displays. WirelessHD is supported by Intel, LG Electronics, Matsushita Electric Industrial (Panasonic), NEC, Samsung Electronics, SiBEAM, Sony and Toshiba. It is expected that the transmitted power will be extremely low (about 10mW or less).

License-free frequency bands around 60GHz have been allocated in Japan, North America (USA/Canada), Korea and Australia (Figure 2). In Europe there is a 59–62GHz band allocated for small-power, short-range device applications; one expects that, if a viable market for 60GHz-band networking develops, this may expand somewhat and that further applications will be developed.

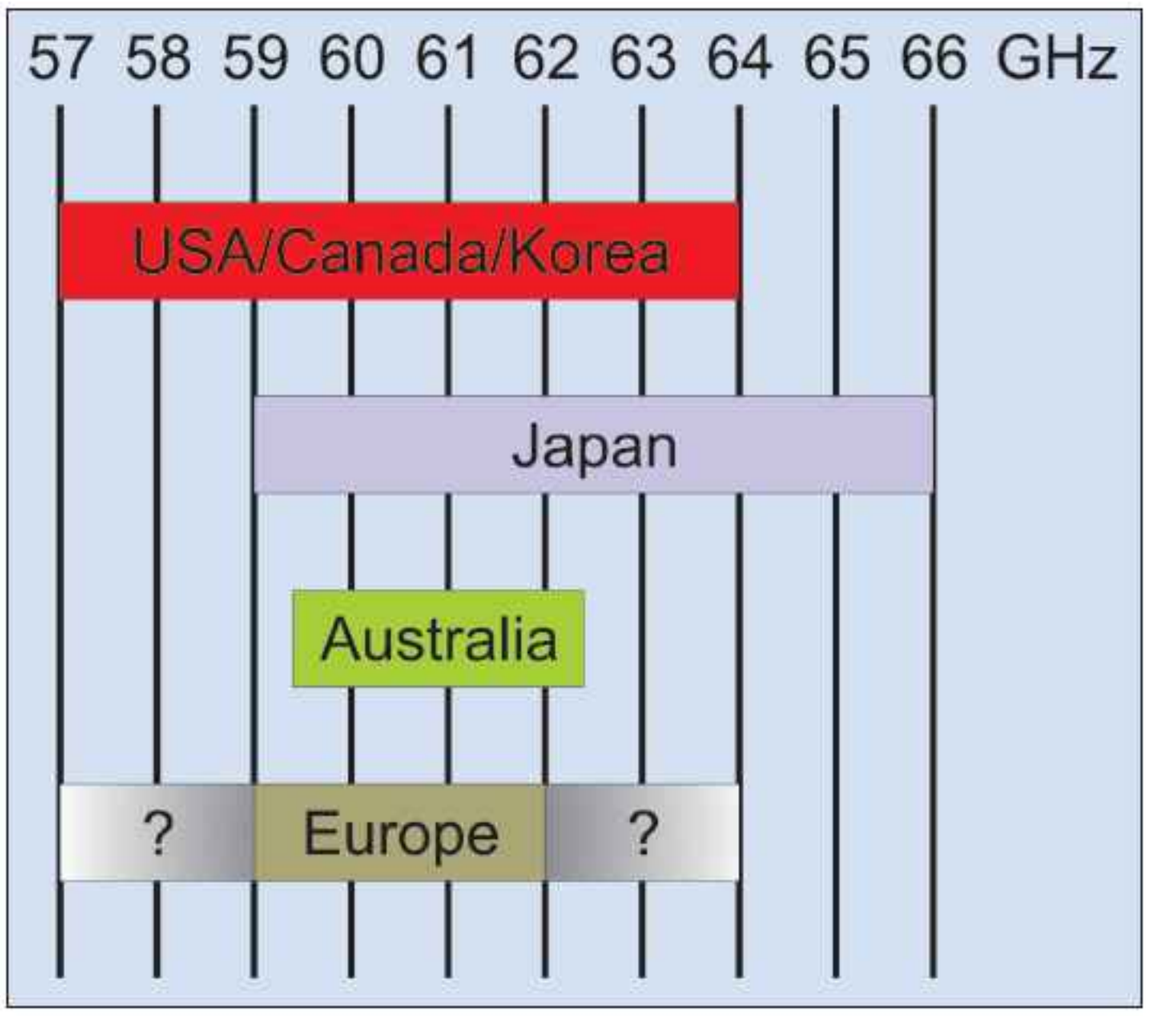

Figure 2. National proposals to use the 60GHz band for WPAN. In Europe, the 59–62GHz band is allocated to small-power, short-range device applications; one expects that, if a viable 60GHz-band networking market emerges, this may expand somewhat.

Another possibility for mm-wave applications is high-resolution measurement using radar techniques, such as in automotive collision avoidance systems. The 77GHz band is used for such applications. In addition, the 95GHz band is used in radar cloud detection, all-weather landing and 'active denial technology' (ADT). ADT radiation penetrates about 0.4mm into skin, causing nonlethal, invisible and inaudible pain (hopefully causing intruders to leave). Such an application would presumably need fairly high powers, putting it outside the scope of possible CMOS applications (for now, at least), apart from control circuits.

The mm-wave space race

Conventional mm-wave circuits mainly use expensive but high-performance compound semiconductor technologies such as gallium arsenide or silicon germanium heterojunction bipolar transistor (HBT) devices. GaAs and other compound semiconductors are also difficult to integrate compactly with digital logic. Compound components operating at tens of gigahertz need to be combined with a number of other parts — including complex antennas, synthesizers, bonding wire, ceramic circuit boards — resulting in time-consuming, expensive and even manual production processes, with yields dependent on the weakest link. The final module is usually large compared to CMOS.

Meanwhile, standard CMOS technology can be highly integrated, with low manufacturing costs starting from

the silicon substrate. CMOS 'scaling' — the development of smaller 'critical dimensions' in ICs — leads to lower costs, lower power consumption and higher frequency, more complex components, and is now entering the mm-wave range in capability. In addition, multiple functions, including digital signal processors (DSPs) can be formed directly on the chip. Therefore it is hoped that one may be able to develop single-chip (or at least fewer chip) circuits and modules capable of converting a digital signal into a 60GHz modulated radio wave and vice versa with fewer assembly problems. The leading drawback is achieving high output power gain while maintaining sufficient long-term reliability.

Ten years ago and more, CMOS scaling was a relatively simple economic and technical process. Signal transmission could be considered almost instantaneous; gate current leakages (leading to power losses and heating) were relatively small. But since devices at the 0.13μm scale entered development (in about 2000), these statements are no longer true; development has become much more difficult and is getting harder.

Extra difficulties arise from the thinner layers, particularly in the gate insulator (traditionally silicon dioxide). These layers are approaching atomic dimensions; to slow this approach, new high-k dielectric materials are being introduced to allow the use of thicker layers. These materials need metal rather than polysilicon gate electrodes, adding to costs. Intel says it has such a metal electrode/high-k insulator gate stack in its latest 45nm production process. The 45nm node is expected to become mainstream for advanced applications in about 2010.

Further reliability problems are expected as the number of atoms across a layer become tens rather than thousands (i.e. the material is no longer 'continuous'). A wide range of potential solutions to these problems are being explored, e.g. channels strained with germanium or consisting of III-V material for higher mobility, new multi-gate transistor structures, silicon-on-insulator, and others.

In addition, the mixing of analog and digital circuitry that is needed for RF applications at tens of gigahertz has a number of further challenges. While pure digital ICs are interested in just two voltage levels, analog devices need smooth reliable performance over a range of voltage and current levels. This performance is deeply affected by issues such as parasitic capacitance and impedance matching to enable maximum signal throughput in amplifiers. If one wants to add DSPs onto analog RF front-end circuitry on one chip, one also has to deal with the noisier digital signals.

CMOS champions

Despite the difficulties, universities and companies around the world are promoting development of CMOS ICs for 60GHz. Examples of progress in this work were presented by a number of organizations at February's International Solid State Circuits Conference (ISSCC 2008) in San Francisco, CA.

Georgia Institute of Technology gave a presentation on a 60GHz single-chip, 90nm CMOS radio integrated with a signal processor that combines analog with multi-gigabit data rates. The super-heterodyne transceiver includes transmit and receive functionality across the 57–66GHz bandwidth. The device supports short-distance (1 meter) data rates up to 15Gb/s, with a total power budget of less than 200mW. At 2 meters 10Gb/s is possible, and at 5 meters 5Gb/s is possible. This is achieved using a quadrature amplitude modulation scheme with 16 'constellation points' (16-QAM). QAM keys the data into two sinusoidal signals (traditionally labeled 'I' and 'Q') that are 90° out of phase. Using quadrature phase-shift keying (QPSK), data rates up to 7Gb/s were achieved. A single-input-single-output (SISO)/multiple-input-multiple-output (MIMO) system was implemented, where user stations use single antennas for transmitting and receiving, while access points use multiple antennas to enable ultra-high data throughput.

The University of California at Berkeley (UCB) contributed three papers at ISSCC 2008 concerning the use of 90nm CMOS for 60GHz, detailing a front-end receiver, a two-stage differential PA and a broadband distributed amplifier.

The 24mW front-end heterodyne receiver has a gain-tuning range of 60dB and an average noise figure (NF) of 6.2dB using a 1V supply. The importance of modeling transistors, coplanar waveguide (CPW) transmission lines, metal-oxide-metal (MOM) capacitors and electromagnetic effects on chips is stressed by the researchers. "Excellent agreement" between measured and simulated performance was found, according to the conference paper.

The differential PA uses compact on-chip transformers for input, output, and inter-stage matching and has an area of 660μmx380μm. On-chip transformers can be used to transform impedances and perform differential-to-single-ended conversion simultaneously with DC biasing. The UCB design uses a 1:1 vertical transformer formed from two coupled loop inductors. It is important to optimize the size of the transformers: too small and the impedance of the shunt magnetizing inductance becomes too small, losing signal current; too big and one finds substrate losses and increased series inductance leakage. Winding diameters of about 50μm are found to be optimum in terms of insertion losses. One PA device that was reported achieves a 1dB compressed output power of 9dBm (7mW) and a saturated power of 12.3dBm (17mW). [Note that power in dBm equates to 10xlog10(power/mW).] The peak drain efficiency is 32% and the peak power-added efficiency (PAE) is 8.8%.

The broadband distributed amplifier uses internal feedback. Applications include high-speed links, broadband radio transceivers, high-resolution radar and imaging systems. The standard digital 90nm CMOS process used to create the broadband distributed amplifier has a cut-off frequency (f_T) of 100GHz operating on a 1.2V supply. The gain-bandwidth product is 660GHz. The 1.19mm^2 chip consumes 84mW.

Also at ISSCC 2008, Belgium's IMEC microelectronics research center and Vrije Universiteit Brussel reported a prototype 60GHz receiver chip for multiple antennas made in a standard digital CMOS process (Figure 3). IMEC has also launched a 60GHz research program to collaborate with industry partners around the world. IMEC used digital CMOS to avoid the costs of alternatives or of a dedicated RF CMOS.

To overcome high path losses at mm-wave frequencies IMEC used a phased antenna array with on-chip programmable phase shifting of incoming signals to allow use of 'beam-forming' to boost reception or transmission in certain directions. The device contains two antenna paths, each consisting of an LNA and a down-conversion mixer. The devices use direct (homodyne) conversion to the digital baseband signal frequency rather than having an intermediate frequency (IF), as in heterodyne conversion. One advantage of homodyne conversion is simpler circuitry, but the technique can limit dynamic range.

The programmable phase shifting starts from the quadrature signals of an on-chip quadrature voltage-controlled oscillator (QVCO). IMEC boasts that its QVCO design combines the highest oscillation frequency with the largest tuning range ever reported in CMOS.

IMEC's multiple antenna receiver is seen as a first step towards a complete CMOS-based phased array transceiver for 60GHz WPANs. IMEC plans to implement four antenna paths using 45nm CMOS technology and to integrate other subsystems such as phase-locked loops (PLL), analog-to-digital converters (ADC) and patch-antenna arrays. IMEC will also begin initial experiments towards power amplifiers.

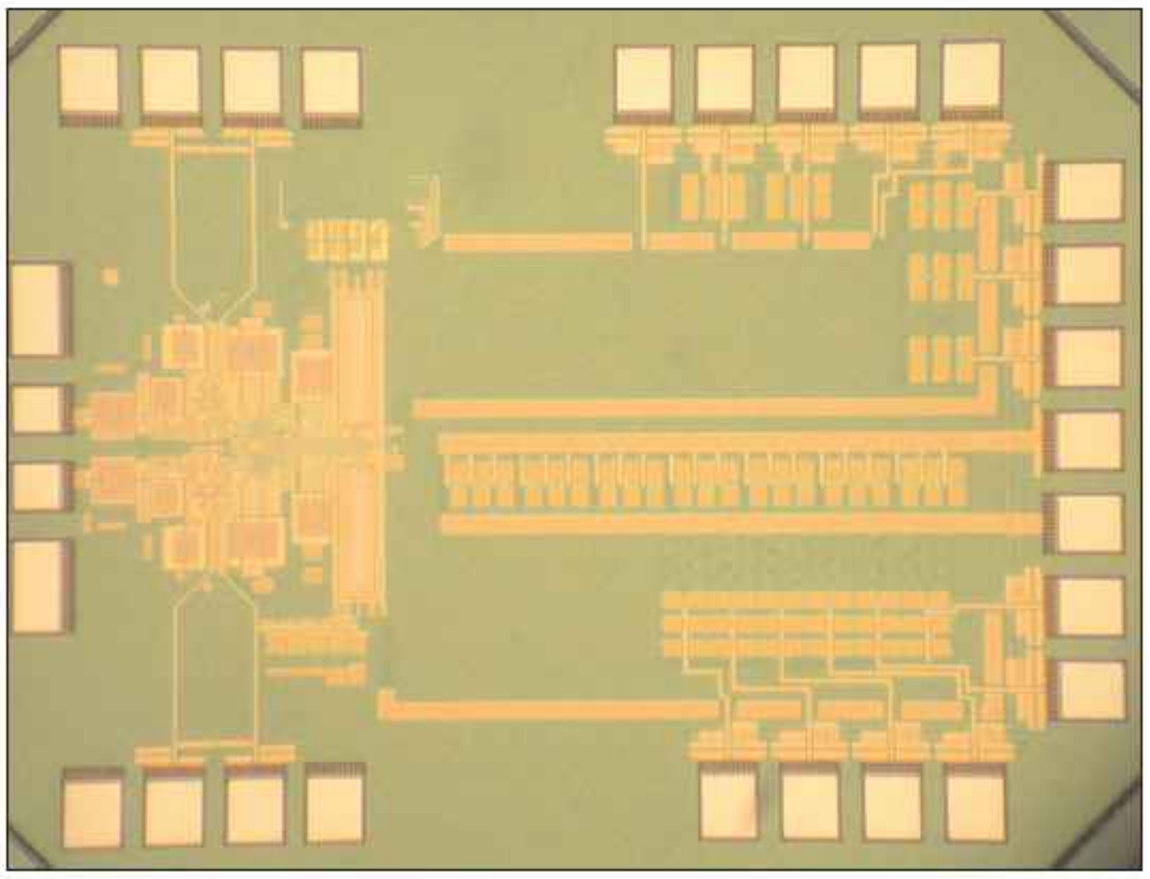

Figure 3. Microphotograph of IMEC's full CMOS multiple antenna receiver for 60GHz (1400x1000µm).

Japan's NEC has developed a two-chip standard 1V 90nm CMOS 60GHz wireless transceiver, claiming the world's highest output power of 7mW. A new design approach maximizes the output power delivered by the power amplifier, while maintaining sufficient long-term reliability, says the firm.

On top of the power amplifier, the transmitter chip contains gain and drive amplifiers and a quadrature modulator, while the receiver consists of two LNAs in series, followed by variable gain (VGA) and driver amplifiers, and then a quadrature (I/Q) demodulator. The complete chip achieves an output power of 6.0dBm (4mW) when it is used with 2.6Gb/s QPSK signals.

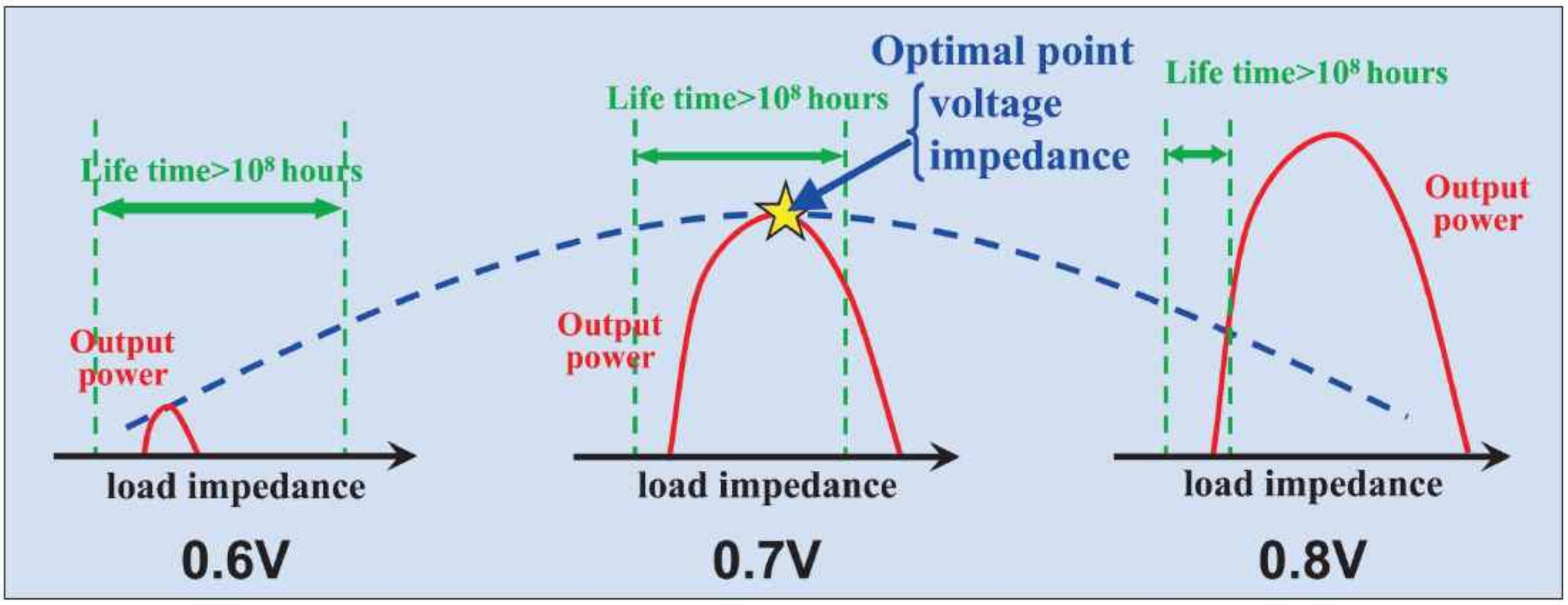

Figure 4. NEC uses co-simulation to maximize reliability and output power with respect to the supply voltage and load impedance.

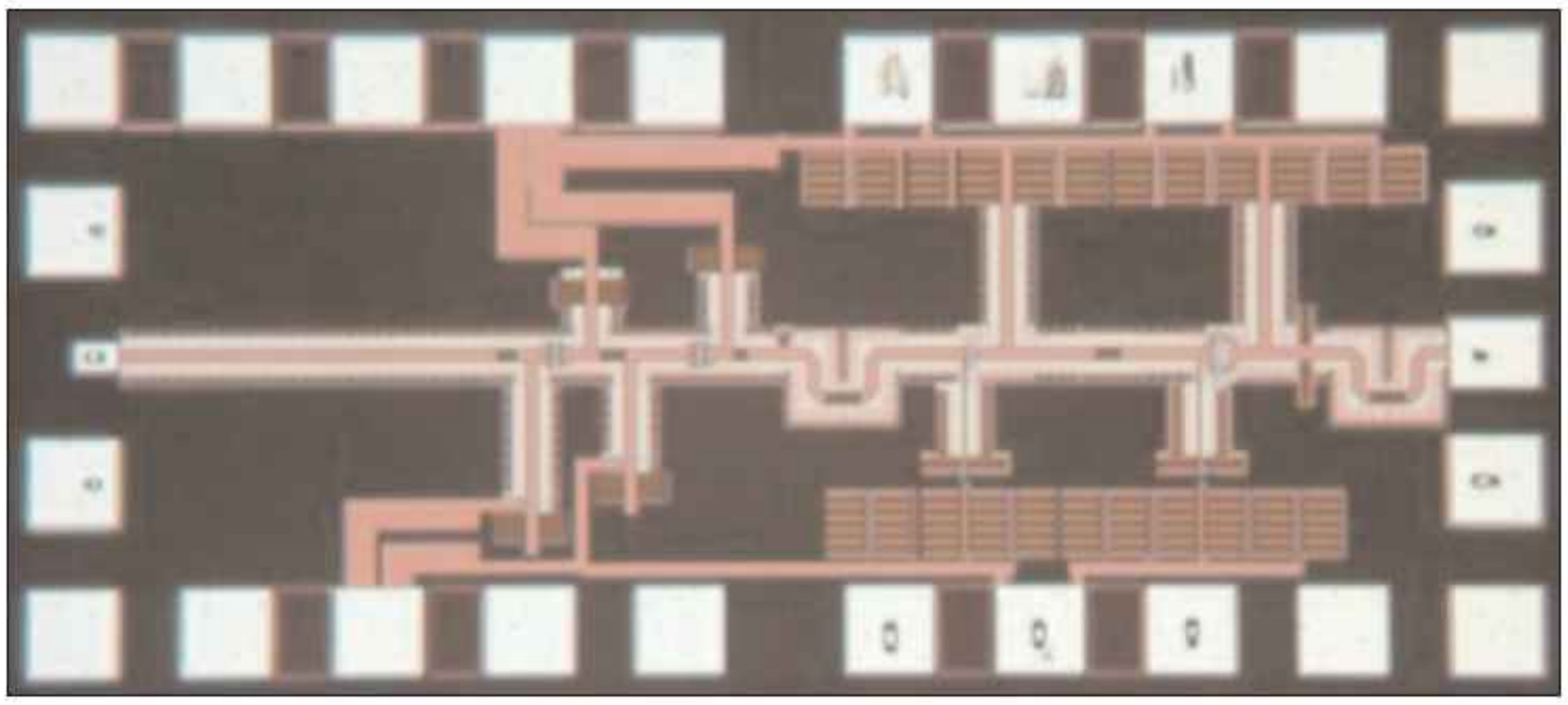

Figure 5. Fujitsu Labs' 77GHz power amplifier chip.

To manufacture the design, NEC performed reliability analyses of CMOS transistors in large-signal operation, to maximize mm-wave output power (Figure 4). The firm says that it will continue the research, with the aim of early commercialization for high-speed wireless solutions in home and office environments, possibly in the next couple of years.

Meanwhile, Fujitsu Labs has developed modeling aimed at minimizing signal loss to develop what it says is the world's first standard 90nm CMOS-based PA to operate at 77GHz (Figure 5). The company is also seeking to produce components for 60GHz wireless communication. The aim is to make a single chip with CMOS radio frequency (CMOS RF) front-end circuitry, including a power amplifier and a baseband DSP.

A short stub matching circuit was integrated with power-supply circuitry to further reduce critical signal losses. A 'short stub' is a short-circuited transmission line where the impedance depends on its length. Short stubs compact the chip area required by the matching circuit to one-tenth of previous levels and reduce signal losses to 0.4dB. The power amplifier operating at 77GHz achieved 8.5dB of gain and 6.3dBm (4.3mW) of saturated output power from a 1.2V supply (Figure 6). Furthermore, a separate power amplifier operating at 60GHz was developed and achieved 8.3dB of gain and 10.6dBm (11.5mW) of saturated output power.

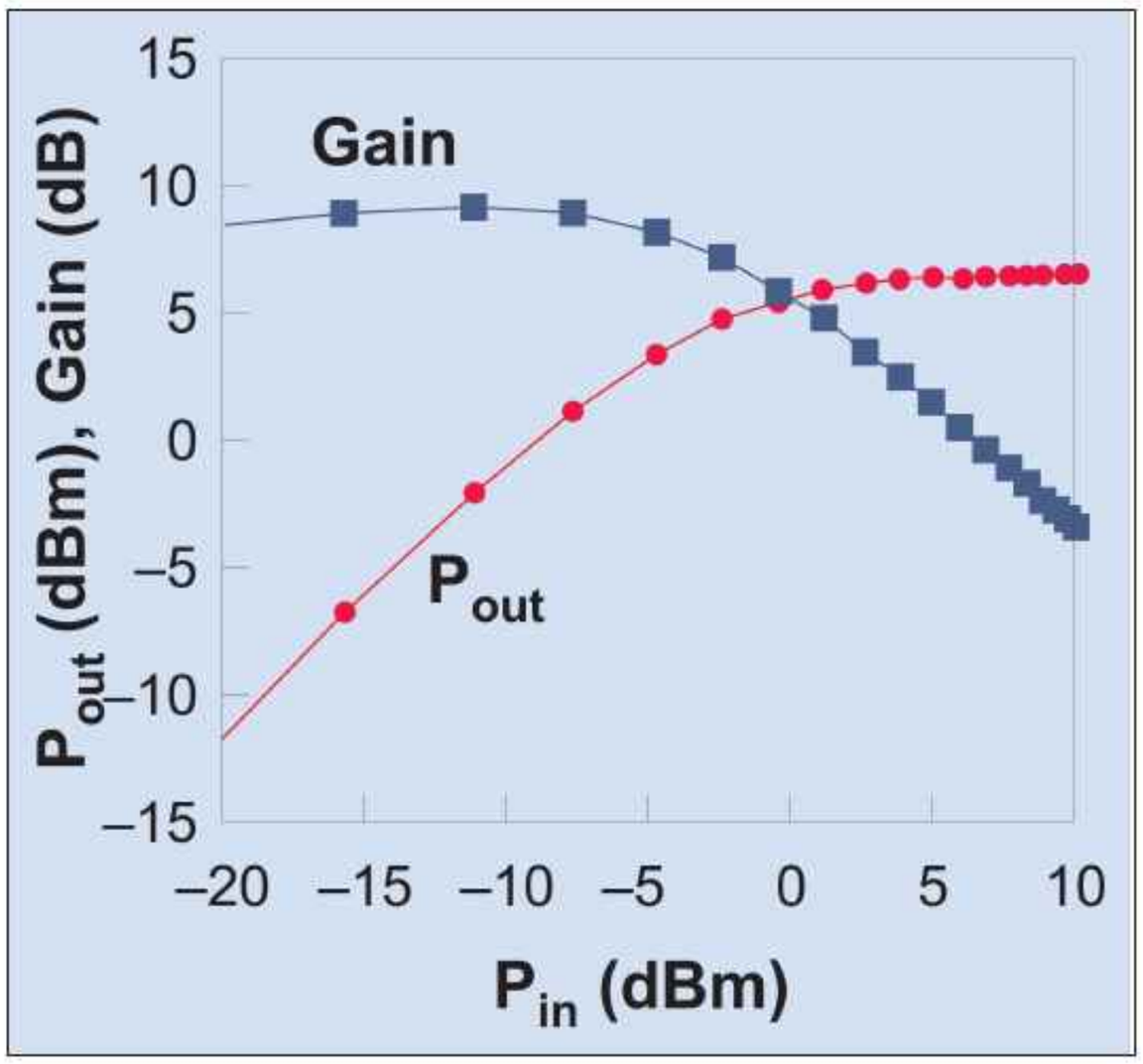

Figure 6. Input-output characteristics for Fujitsu Labs' 77GHz PA. The peak gain is measured as 8.5dB and the peak output power 6.3dBm (4.3mW).

The University of Toronto, with help from STMicroelectronics, has developed a fully integrated 76–95GHz band receiver produced in 65nm digital CMOS. The researchers are seeking to develop technologies for double-sideband imaging, remote sensing and 10Gb/s communication. Further motivation is to explore the capabilities of advanced CMOS. Beyond 65nm, the researchers expect 45nm devices to handle 120GHz RF communications, and 32nm to handle 160GHz.

The 65nm transistor that was used has cut-off frequencies of 170GHz for f_T and 250GHz for f_{max}. The receiver includes an LNA, mixer, IF amplifier, fundamental-frequency VCO with buffers, and divider with 50Ω driver, all consuming 206mW. Operation up to 100°C was shown. The conversion gain is 12.5dB and NF is 7dB.

The University of California, Los Angeles reported on a 60GHz 36mW double-conversion heterodyne receiver using a 30GHz local oscillator fabricated in 90nm CMOS. The receiver achieves NFs of 5.7–8.8dB and gains of 18.3–22dB. Ruhr-Universität Bochum presented on a 60GHz 65nm CMOS 35mW LNA with single-ended input and differential outputs with 22.3dB voltage gain and NF of 6.1dB. The chip occupied 0.46mm x 0.46mm.

Although ISSCC 2008 presented a cross-section of ongoing work to develop tens of GHz RF CMOS, there were some notable absences. Toshiba is also working in this area. In 2007, it announced a low-cost 90nm CMOS process to achieve high-speed, highly integrated wireless communications over short distances for consumer applications, unveiling the technology at the VLSI Circuits symposium in Kyoto. It has realized a 60GHz CMOS receiver chip integrating an on-chip antenna, LNA, mixer with preamplifier and phase-locked loop (PLL) synthesizer in a die of 1.1mm x 2.4mm without pad areas. Toshiba believes its 90nm process achieves a performance close to that of GaAs devices. Element and wiring structures are optimized to restrain internal noise for stable operation. Beyond improving the receiver circuit, Toshiba plans to develop the high power required for a transmitter IC, aiming to achieve a practical mm-wave CMOS transceiver "at an early date". ■